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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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WOERNER & KELTH, P.
1200 12th Street
YUCCA, CALIFORNIA

EXAMINER

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)
	09/620,679	RUESCH, RODNEY
	Examiner	Art Unit
	Don P Le	2819

-- The MAILING DATE of this communication app ers on the cov rsh et with the correspondenc address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
 THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 23 July 2001.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) 1-6 and 17-22 is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 7-10,15,16 and 23-25 is/are rejected.

7) Claim(s) 11-14 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>3-6</u> .	6) <input type="checkbox"/> Other: _____

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 7 and 23-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Knee et al. (US 5,337,254).
3. With respect to claim 7, figures 1-4 of Knee teaches a method of communicating data in an integrated circuit using internal interconnects, the method comprising:

receiving a data signal (100);

adjusting a first resistance (transistor 1X connected to VDD at 110) coupled to a first supply voltage (VDD), based on a manufacturing process, the first supply voltage and a temperature (PVT control signal from 18 through microprocessor to 70);

adjusting a second resistance (transistor 1X connected to ground at 110) coupled to a second supply voltage (ground), based on the manufacturing process,

the first supply voltage and the temperature (PVT control signal from 18 through microprocessor to 70); and

adjusting a third resistance (transistor 2X connected to ground at 112) coupled to the second supply voltage (ground), based on the manufacturing process, the first supply voltage and a temperature (PVT control signal from 18 through microprocessor to 72).

4. With respect to claim 23, figure 3 of Knee teaches adjusting a first resistance (1X of 110) includes changing a resistance of a semiconductor.

5. With respect to claim 24, figure 3 of Knee teaches adjusting a first resistance includes changing a gate voltage on a field effect transistor (FET).

6. With respect to claim 25, figure 1 of Knee teaches selecting a predetermined number of programmable bits from a plurality of programmable bits (microprocessor provides bits to 16 to control the resistance.)

7. Claims 8-10, 15, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Esch, Jr. (US 6,118,310).

8. With respect to claim 8, figures 4-6 of Esch teaches a method of communicating data in an integrated circuit using internal interconnections, the method comprising:

selecting a resistance of a divider network (262, 264 of figure 6) based on a manufacturing process, a supply voltage and a temperature;

selecting an edge rate of a driver (edge rate is controlled by 266) coupled to the divider network, the selected edge rate based on the manufacturing process, the supply voltage and the temperature;

receiving a data signal (203); and

providing an output (output at 241) based on the data signal, the resistance, and the edge rate.

8. With respect to claim 9, figure 6 of Esch teaches selecting an edge rate of a driver coupled to the divider network comprises maintaining a substantially constant edge rate.

10. With respect to claim 10, figure 5 of Esch teaches providing an output turning on a PFET transistor (212) and turning off an NFET transistor (222).

11. With respect to claim 15, figure 5 of Esch discloses the step of receiving a tristate enable signal (ENABLE); and actuating a switchable resistance element (230) in response to the tristate enable signal.

12. With respect to claim 16, figure 5 of Esch discloses actuating a switchable resistance element comprises actuating a programmable inverter (230 configured as inverter).

Allowable Subject Matter

13. Claims 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is an examiner's statement of reasons for allowance:

With respect to claim 11, in addition to other elements in the claim, the prior art does not teach a method of communicating data having a step of selecting a resistance of a divider network comprises selecting a plurality of parallel resistance elements.

With respect to claim 12, in addition to other elements in the claim, the prior art does not teach a method of communicating data having a step of selecting a resistance of a divider network comprises executing programming for selecting resistance elements from a plurality of switchable resistance elements.

With respect to claim 11, in addition to other elements in the claim, the prior art does not teach a method of communicating data having a step of selecting an edge rate of a driver coupled to a divider network comprises programming for selecting resistance elements from a parallel resistance elements.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

15. Applicant argues that restriction as per Office Action dated 6/20/2001 was improper because examiner did not provide example of how the process of claims 7-16, 23 and 25 could be practiced using a product materially different from that of

claims 1-6, and 17-22. The rejections of the process claimed by applicant above show that the process as claimed could be applied to other products different than that disclosed by applicant (Knee and Esch references). Therefore, the restriction is proper. **Restriction is final.**

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a. Thayer et al. (US 5,598,119) discloses a PVT driver circuit.
- b. Pollacheck (US 6,051,995) discloses a PVT driver circuit.
- c. Vishwanthaiah et al. (US 6,060,907) discloses a PVT driver circuit.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P Le whose telephone number is 703-308-4890. The examiner can normally be reached on 7AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J Tokar can be reached on 703-305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

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Art Unit: 2819

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Don Phu le
October 4, 2001